REMARKS

Claims 1-20 are pending in the present applicant for invention. Claims 1 and 7 are independent.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,502,512 (*Toyoda*) in view of US Patent No 5,923,892 (*Levy*).

Claim 1 recites, *inter alia*, a multi-processor unit, including, "first domain processing means for first processing the data depending on first domain configuration information," "the first domain processing means including multiple first domain processors," "each first domain processor differently sub-processing the data in order to first process the data," and "the first domain processors including a first domain control processor for controlling the first processing of the first domain."

Claim 1 further recites "second domain processing means for second processing the first processed data depending on second domain configuration information," "the second domain processing means including multiple second domain processors," "each second domain processor differently sub-processing the data in order to second process the data," and "the second domain processors including a second domain control processor for controlling the second processing of the second domain."

Claim 1 further recites "a global control processor ... for providing the first domain configuration information and the second domain configuration information through the communication means for configuring the first and second domains."

Importantly, claim 1 recites a patentable combination of the above-described features. Thus, claim 1 recites a multi-processor unit wherein a "first domain processing means" in combination with a "second domain processing means." The "first domain processing means" includes "multiple first domain processors," and the "second domain processing means" includes "multiple second domain processors." Each first domain processor "differently" sub-processes the data. Each second domain processor "differently" sub-processes the data. In addition, a "first domain control processor" is included among the first domain processors, while a "second domain control processor" is included among the second domain processors. Separately, claim 1 recites a "global

control processor" that provides first domain configuration information and second domain configuration information ... for configuring the first and second domains.

Thus, claim 1 recites a specific combination of components is a specific architecture to beneficially channel decoding.

Applicant submits that neither *Toyoda* nor *Levy*, either taken alone, or in combination, teach, describe or provide motivation for the patentable combination of features recited by claim 1.

Toyoda describes a digital audio and video processing system that includes multiple processing means 101, 102, a control means 105, input means 106 and bus means 107. *Toyoda* does not, however, describe the patentable combination of features of claim 1.

For example, if, for sake of argument, the means 101 and means 102 of *Toyoda* are considered to be first and second "domain processing means," as asserted in the Office Action, *Toyoda* does not describe "first domain processing means for first processing the data depending on first domain configuration information" and "second domain processing means for second processing the data depending on second domain configuration information."

In addition, if, for sake of argument, the means 101 and means 102 of *Toyoda* are considered to be first and second "domain processing means," as asserted in the Office Action, *Toyoda* does not describe "the first domain processing means including multiple first domain processors," and "the second domain processing means including multiple second domain processors."

In addition, if, for sake of argument, the means 101 and means 102 of Toyoda are considered to be first and second "domain processing means," as asserted in the Office Action, *Toyoda* does not describe "each first domain processor differently sub-processing the data in order to first process the data," and "each second domain processor differently sub-processing the data in order to second process the data."

Moreover, *Toyoda* does not describe the patentable combination of the above-described features, but merely a combination processors that process audio and video data.

Levy does not make up for the deficiencies of *Toyoda*. While *Levy* describes a host processor and coprocessor arrangement for processing, *Levy* does not describe the claimed combination of "first domain processing means for first processing the data depending on first domain configuration information" and "second domain processing means for second processing the data depending on second domain configuration information."

In addition, *Levy* does not describe "the first domain processing means including multiple first domain processors," and "the second domain processing means including multiple second domain processors."

Further, *Levy* does not describe "each first domain processor differently sub-processing the data in order to first process the data," and "each second domain processor differently sub-processing the data in order to second process the data."

Moreover, no description, teaching, or motivation is provided by any proposed combination of *Toyoda* and *Levy* for these combination of features recited by claim 1.

In addition, if, for sake of argument, the processor and coprocessor arrangement of *Levy* were considered to be a "domain" having multiple processors, as asserted in the Office Action, neither *Toyoda* nor *Levy*, either alone, or in combination, describe, teach or provide motivation for features recited by claim 1, such as, for example, "first domain processing means for first processing the data depending on first domain configuration information" and "second domain processing means for second processing the data depending on second domain configuration information"; "the first domain processing means including multiple first domain processors," and "the second domain processing means including multiple second domain processors"; and "each first domain processor differently sub-processing the data in order to first process the data," and "each second domain processor differently sub-processing the data in order to second process the data."

Accordingly, for the foregoing reasons, this rejection is, respectfully, traversed.

Claims 2 and 7-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Toyoda in view Levy, further in view of U.S. Patent Publication No. 2003/0032390 (Geile) and further in view of US Patent No 5,844,941 (Macket).

First, claims 2 and 16-20 depend from claim 1, that has been previously discussed, and are believed to be allowable and further narrow and define claim 1. Therefore, claims 2 and 16-20 are also believed to be allowable.

Second, regarding claims 2 and 7, the rejection asserts that claimed limitations of "the communication means include a stream-based communication means connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting
information streams between connected processors" and "the stream-based communications means are connected to an input/output bus to at times receive stream of data into the multi-processor unit through the stream-based communications means in to one of the connected processors and to at other times transmit a stream of data from one of the connected processors through the stream-based communications means onto the input/output bus" are met by the bus means 107 within Figure 1 of *Toyoda* The Applicant does not concur with this assertion. *Toyoda* do not disclose, or suggest, the subject matter for the communication means include a stream-based communication means connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors.

The Examiner admits that the combination fails to disclose blocks of memory with selective interconnections to the plurality of processors. The rejection alleges that *Levy* teaches block of memory with selective interconnection to a plurality of processors at col. 7, line 61-col. 8, line 20. The Applicant disagrees. *Levy* simply discuses that memory transfers that are handled via DMA. There is no disclosure or suggestion for blocks of memory with selective interconnections to the plurality of processors within *Levy*.

The applicant respectfully points out that Claims 2 and 7 define subject matter for a multi-processor unit that includes blocks of electronic memory, the communication means includes block-based communication means connected to the processors and a processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block. This subject matter is not disclosed or suggested by the cited prior art references.

The rejection admits that the combined teaching of *Toyoda* with *Levy* fails to disclose that *Geile* the processing includes FFT and IFFT processing. The Examiner alleges that *Geile* teaches FFT and IFFT processing. The Applicant points out that Claim 2 defines that the processing of the first domain includes FFT and IFFT. There is no disclosure or suggestion that the processing of the first domain within a multi-domain multi-processing unit includes FFT and IFFT within *Geile*.

The rejection admits that the combined teaching of *Toyoda* with *Levy* fails to disclose the use of a periodic sequencer. The rejection alleges that *Geile* teaches periodic processing. The Applicant points out that Claim 2 defines that "at least one of the domain processors includes a periodic sequencer". This subject matter is not disclosed or suggested by the combination of *Toyoda* with *Levy*, *Geile* and *Macket* The rejection only finds a sequencer, which alone does not address the foregoing subject matter.

The applicant, respectfully points out that Claim 2 defines subject matter for at least one of the domain control processors includes a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter. The rejection alleges that the combination of *Toyoda* with *Levy*, *Geile* and *Macket* teaches a periodic sequencer. Specifically, the Examiner states that *Macket* at col. 8, line 60-col. 9, line 28 teach equalization of a stored received signal for reconstruction. The Applicant assert that this allegation does not reach the subject matter for at least one of the domain control processors includes a

periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter.

In view of the aforesaid reasons and arguments, this rejection is traversed.

Claims 3-6 stand rejected under 35 U. S. C. 103(a) as being unpatentable over Toyoda with Levy and further in view of Integrated Circuits and Microprocessors by R.C. Holland (Holland). Claims 3-6 depend from claims that have been previously discussed and are believed to be allowable and further narrow and define these claims. Therefore, Claims 3-6 are also believed to be allowable.

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CONCLUSION

In view of the above remarks and amendments, reconsideration and allowance of the present application is respectfully requested. The Commissioner is hereby authorized to charge the fee for a one-month petition for extension of time to Deposit Account No. 50-1358.

Respectfully submitted,

Paul Im
Registration No. 50,418

By: James Dobrow
Attorney for Applicant
Registration No. 46,666

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Mail all correspondence to:
Paul Im, Registration No. 50,418
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9627
Fax: (914) 332-0615

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James Dobrow, Reg. No. 46,666
(Name of Registered Rep.)

18 SEPT. 2006
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